Instantly Available PC

System Power Delivery Requirements and Recommendations

(A.K.A POWER SUPPLY '98)

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1. INTRODUCTION

System-wide improvements in desktop PC power management technology, enabled by Intel's Instantly Available PC architecture, place new requirements on the PC's power delivery subsystem.

The single most important capability that this specification calls out is Suspend to RAM (STR). STR enables the PC, using self refreshed DRAM instead of the hard disk, to save and restore system state in seconds with very low power consumption while in the "off" (sleeping) state. STR enables a noiseless sleeping PC that resumes normal operation in a matter of seconds on demand, and which can remain connected to a modem or LAN even when "off".

The features required for support of STR, and in a more general sense the Instantly Available PC, include a 3.3Vstby output, Dual Mode Voltage Output(s), Dual Mode Voltage Output control, and fan speed control.

1.1. SCOPE

This document is intended to describe a list of power delivery capabilities that enable the construction of an Instantly Available PC. This document is not a power supply product specification. The capabilities described herein may be implemented in a distributed manner using existing power supplies with motherboard hardware assist for example, or they could be tightly integrated into new power supply designs. The system manufacturer can choose which level of integration vs. distribution of functionality makes the best business/technical sense for themselves.

Beyond specifying the minimum set of requirements, additional recommendations are presented as a means of tapping architectural headroom such as enabling more wake devices in the system, for example.

2. ELECTRICAL SPECIFICATION

2.1. CONTROL SIGNALS

2.1.1. REMOTE SENSE

To allow for better voltage regulation a remote sense lines have been defined for the main +3.3 Vdc and +3.3 Vdual outputs. The remote sense is used to compensate for voltage drops in the wiring harness and connector.

2.1.2. POWER ON SIGNAL

PS-ON# is a control signal generated by a motherboard (ACPI controller) to turn on the main power converter.
PS-ON# is an active low control input to the power delivery subsystem. PS-ON# turns on the +3.3 Vdc, +5 Vdc, +12 Vdc, and -12 Vdc outputs. When this signal is held high by the PC motherboard, or is open circuit, the main power converter shall be held in the standby mode of operation and the +3.3 Vdc, +5 Vdc, +12 Vdc, and -12 Vdc outputs shall be at zero volts. The operation of the +3.3 Vdual and +5 Vdual outputs is defined in Section 2.1.3.1 . The PS-ON# signal shall have no affect on the +3.3 Vsby output. The PS-ON# is a +3.3V signal however the input buffer must be +5V tolerant to allow for 5 V TTL logic.

2.1.3. DUAL POWER ON SIGNAL

DUAL-ON# is an active low control input to the power delivery subsystem. When DUAL-ON# is active (low) the +3.3 Vdual and +5 Vdual outputs are configured for their normal mode of operation. When DUAL-ON# is held high (inactive) by the ACPI controller, or is open circuit, the dual outputs shall be at zero volts. The operation of the +3.3 Vdual and +5 Vdual outputs is defined in Section 2.1.3.1. The DUAL-ON# signal shall have no effect on the +3.3 Vsby output. The DUAL-ON# signal is a +3.3V signal however the power delivery subsystem input buffer must be +5V tolerant.

The Dual Power ON (DUAL-ON#) signal is recommended for systems that wish to turn off both main and dual converters (e.g. in support of ACPI's S5 "soft off" state). When both PS-ON# and DUAL-ON# signals are high, the only active output is 3.3Vstby. 3.3Vstby is connected to the motherboard's ACPI controller and to the suspend/resume button. Keeping these subsystems powered enables the system to be turned on from the "Soft Off" S5 state. Note that all power to the wakeup devices is removed when DUAL-ON# is high.

2.1.3.1. Vdual OUTPUTS

The +3.3 Vdual, and +5 Vdual outputs are controlled by the PS-ON# and DUAL-ON# signals specified in the Section 2.1.2 and Section 2.1.3. The operation of the dual mode outputs is described in the Table 1.

A fault on either the +3.3 Vdual or +5 Vdual output, sensed as either an over current condition or an under voltage condition, shall cause the dual outputs to be turned off.

Table 1. Power delivery subsystem Operating States.

PS-ON#	DUAL-ON#	Conditions	Standby Outputs	Dual Outputs	Main Outputs
1	1	Soft OFF state	ON	OFF	OFF
1	0	Suspend state	ON	ON (low capacity output current)	OFF
0	X	Normal operation	ON	ON (high capacity output current)	ON

0 - indicates voltage level low.
1 - indicates voltage level high. It can be either +3.3V or +5V.

X - indicates that it can be either 0 or 1

2.1.4. MAIN POWER GOOD SIGNAL

PW-OK is an active high signal that shall be asserted (high) by the power delivery subsystem to indicate that the +5 Vdc and +3.3 Vdc outputs are above the under-voltage thresholds of the power delivery subsystem. When this signal is asserted (high), there shall be sufficient mains energy stored by the power delivery subsystem to guarantee full power continuous operation within specification for the time period specified in Section 2.3.5. Conversely, when either the +5 Vdc or +3.3 Vdc output voltage falls below the under-voltage threshold, or when mains power has been removed for a time sufficiently long so that power delivery subsystem operation is no longer guaranteed, PW-OK shall be deasserted (driven, and held low). See Section 2.1.6 for a representation of the timing characteristics of the PW-OK and PS-ON# signals and representative output voltages. PW-OK is an open collector output which requires a 10K-ohm pull-up resistor external to the power delivery subsystem.

Note that PW-OK will be activated every time the system is powered up, either for the first time or when it resumes from a sleep state, and therefore PW-OK cannot be used to initialize or reset the wakeup devices or the memory controller.

2.1.5. DUAL POWER GOOD SIGNAL

DLPW-OK is a “power good” signal that is activated (driven high) by the power delivery subsystem to indicate that the +3.3 Vdual and +5 Vdual outputs are above the under-voltage threshold of the power delivery subsystem. DLPW-OK follows the same definition as that of the PW-OK signal, with the only difference being that it relates to the status of the dual mode voltage outputs. This signal can be used to reset wakeup logic on the motherboard or the memory controller. DLPW-OK will be activated only when AC power is initially applied to the system. This signal will not be activated when the system resumes from a sleep state.

When DLPW-OK is asserted high, there shall be sufficient mains energy stored by the converter to guarantee full power continuous operation within specification for the time period specified in Section 2.3.5. Conversely, when either the +3.3 Vdual or the +5 Vdual output fall below the under-voltage threshold, or when mains power has been removed for a time sufficiently long so that operation is no longer guaranteed, DLPW-OK shall be deactivated (driven low). DLPW-OK is open collector signal and requires a 10K-ohm pull-up resistor to +3.3 Vsby external to the power delivery subsystem.

2.1.6. SIGNAL TIMING

Figure 1 details the signal timing for main power connector signals and rails. This figure applies to PW-OK for all transitions of the PS-ON# signal and it applies to DLPW-OK for initial turn-on of the Vdual output voltages. It is not required for the DLPW-OK signal to transition to inactive state before dual outputs. (T4 timing of Figure 1 does not need to be met for DLPW-OK signal)

It is recommended that the power delivery subsystem minimize the time between PS-ON# active to PW-OK valid. Reducing this time will reduce the overall system resume latency.

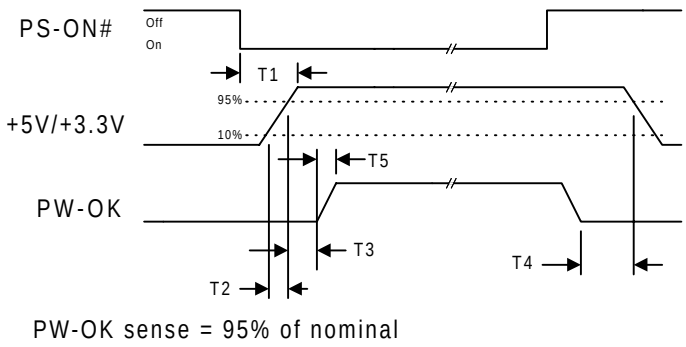

Figure 1. Timing of PS-ON#, PW-OK, and Germane Voltage Rails

Symbol	Description	Min	Nom	Max	Unit
T1	Turn on delay			1	Sec.
T2	10%-95% voltage ramp rate	2		200	mSec
T3	95% voltage to PW-OK delay	50		500	mSec
T4	PWR-OK inactive to <95% Voltage	1			mSec
T5	PWR-OK rise time			1	mSec

2.1.7. FAN SPEED CONTROL SIGNAL

Programmable fan speed is essential to the Instantly Available PC. This capability enables the presentation of a completely silent low power sleep state. Two commonly used schemes for controlling fan speed are:

- Linear voltage control
- Pulse width modulation (PWM)

Pulse width modulation allows more flexibility for the system designer and allows finer fan speed granularity. A PWM controlled fan support may also be less expensive to implement than support of a linear voltage controlled fan which would require the use of a Digital to Analog converter (DAC).

The following are the recommended attributes for a PWM controlled fan system.

Fan speed is controlled by a pulse width modulated control signal (FANCON). FANCON controls the fan's speed by modulating its on/off duty cycle, and has a control range of 20% to 100% of rated fan speed. FANCON is a 3.3V signal (0V = off, 3.3V = on). If the system designer does not implement fan speed control, yet the system's power delivery subsystem comprehends fan speed control, he must ensure that the fan runs at full speed whenever the system is powered. This could be done by deploying a pull up resistor on the FANCON power delivery subsystem's input. The FANCON input must be capable of accepting an input voltage as great as +12Vdc without damage, and this input shall cause the fan to run at maximum speed.

2.1.8. FANRPM SIGNAL

The FANRPM signal is used for early detection of a fan failure which could lead to thermally related system failures. This control signal is supplied by the power delivery subsystem to the motherboard. It is an open collector, 2 pulse per revolution tachometer signal from the power delivery subsystem fan. The signal stops cycling during a locked rotor state; the level can be either high or low. Implementation of this signal allows a system designer to gracefully power down the system in the event of a critical fan failure. The monitoring circuit on the motherboard uses a 1k-10k Ohm pull up resistor to +3.3 Vdc for this signal.

2.1.9. FAN SPEED CONTROL OVERRIDE

The fan speed control mechanism should be treated by the power delivery subsystem as a request and shall be overridden by the power delivery subsystem if the temperature in the power delivery subsystem should exceed 52.5 +/- 2.5 degrees Celsius. In this case the power delivery subsystem shall operate the fan at its maximum speed until the temperature drops below 42.5 +/-2.5 degrees. The fan speed shall then return to the speed set by the fan speed control mechanism.

2.2. AC INPUT RECOMENDATIONS

The power delivery subsystem should support two input voltage ranges for continuous operation, rated 100-120 Vac and 200-240 Vac RMS. The input voltage and frequency recommendations for continuous operation are stated below. The input voltage range may be selectable between the two ranges. Note that nominal voltages for test purposes are considered to be within ±1.0 V of nominal.

Table 2. AC Input Recommendations

Parameter	Minimum	Nominal	Maximum	Unit
100-120 Vac	90	115	132	Vac rms
200-240 Vac	180	230	264	Vac rms
Vac Frequency	47	-	63	Hz

2.2.1. INPUT OVER CURRENT PROTECTION

The power delivery subsystem should incorporate primary fusing for input over current protection. A slow blow fuse is recommended.

2.2.2. INRUSH CURRENT LIMITING

Repetitive ON/OFF cycling of the AC input voltage shall not damage the power delivery subsystem. Half cycle peak inrush current, peak repetitive input current, and worst case power factor data should be provided to assist with UPS and line conditioning sizing and selection.

2.2.3. LINE TRANSIENTS

2.2.3.1. SLOW TRANSIENTS

The DC outputs should not exceed the limits specified in Section 2.3.2 as a result of input power line noise as defined in Table 3. In addition, the sag, surge and dropout from standard TC110 as specified in Table 4 should be met.

The Table 4 input voltage is referenced to the 230 VAC, 50 Hz nominal line.

Table 3. Line Voltage Transient Limits:

TRANSIENT EVENT AT THE NOMINAL INPUT LINE FREQUENCY	TYPE	AMPLITUDE RELATIVE TO AC LINE
50 ms-500 ms DURATION	SURGE	+10% above 120/240 Vac
50 ms-500 ms DURATION	SAG	-10% below 100/200 Vac
0.5 ms-10 ms DURATION	SAG	-100% below 100/200 Vac
0.5 ms-8.33 ms DURATION	SURGE	+30% above 120/240 Vac

Note: The power delivery subsystem shall be loaded to 50% of the maximum load specified in Section 2.3.1

Table 4. TC110 Standard Recommendations.

TEST EVENT FROM NOMINAL 230 Vac, 50 Hz	DURATION	PERFORMANCE CRITERIA
15% SAG (195.5 Vac, 50 Hz)	15 Min.	No loss of func. or perf.
30% SAG (161.0 Vac, 50 Hz)	10 ms	No loss of func. or perf.
50% SAG (115.0 Vac, 50 Hz)	100 ms	Loss of function allowed, self-recoverable
DROPOUT (0.0 Vac)	500 ms	Loss of function allowed, self-recoverable
10% SURGE	15 Min.	No loss of func. or perf.

Note: The recommended loading of the power delivery subsystem is 50% of the maximum load specified in Section 2.3.1. The power delivery subsystem should be able to operate in a worldwide environment. The transient conditions in this environment may exceed the applicable standard recommendations as specified in Table 4 above. The vendor should provide recommendations for additional transient limits for the power supply.

2.2.3.2. FAST TRANSIENTS

The power delivery subsystem should meet the IEEE Standard 587-1980 for surge withstand capability under categories A and B, with the following conditions and exceptions;

- The crest value of the first half peak of the injected oscillatory wave will be 3.3K volts open circuit with 200 and 500 Ampere short circuit current for the common and the normal modes of transient surge injection, respectively.

- The peak value of the injected unipolar wave form shall be 1.5 KV to 2.0 KV measured at the input of the power supply for the common and the normal modes of transient surge injection.

The power delivery subsystem should meet the surge withstand test for the environmental conditions of operation specified below. The surge withstand test must not produce damage to the power delivery subsystem, disrupt the normal operation of the power delivery subsystem, nor cause the outputs deviate more than ± 5% from nominal voltage. Figure 2 below shows the test setup for the surge withstand test.

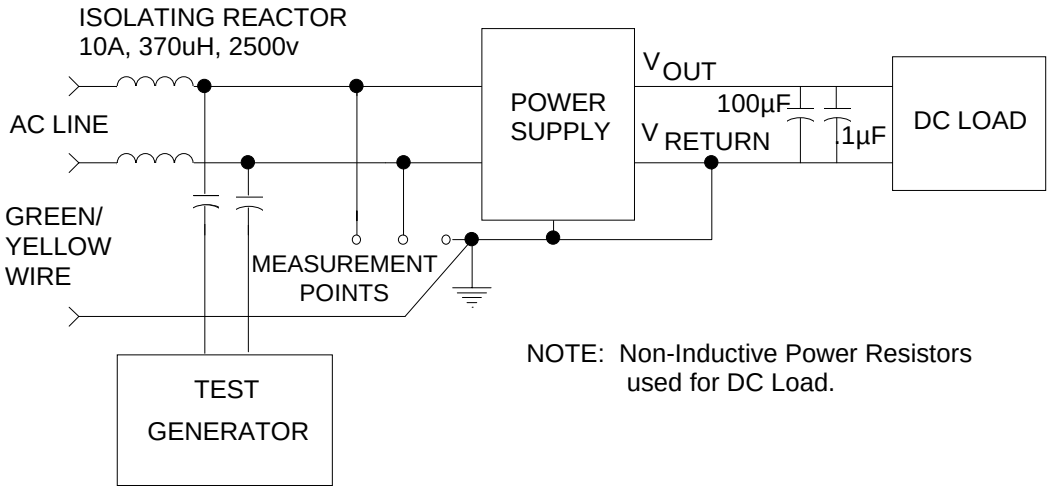

Figure 2. Input Surge Withstand Test Block Diagram.

2.2.4. HARMONIC CURRENT LIMITATIONS

This feature is optional. If supported, the power delivery subsystem should meet the harmonic current distortion requirements set forth in IEC Publication 1000-3-2, limits for harmonic current emissions.

2.3. DC OUTPUT REQUIREMENTS AND RECOMMENDATIONS

In the normal mode of operation, all outputs, main, dual mode and standby, are available at full output current. In the standby mode of operation, the +3.3 Vsby standby output is present so long as the power delivery subsystem is connected to a source of AC voltage as defined in Section 2.2 The dual mode outputs, +3.3 Vdual and +5 Vdual (if supported), may or may not be present during standby operation depending upon the dual mode output control. Only a small amount of power is available on the dual mode outputs in the standby mode. The dual mode outputs are intended to support Suspend to RAM (STR) and the I/O bus wakeup features of the desktop platform.

2.3.1. DC OUTPUT CURRENT

The DC output load currents are shown in the tables below. These tables show maximum and minimum loads for both normal and standby modes of operation. The minimum load currents shown in Table 5 for the normal operating mode are the values expected during the transition from

normal mode to standby mode and back. Regulation on all outputs must be maintained during these transitions. Standby Mode loading corresponds to the case where the dual mode outputs route the auxiliary power source out. Normal Mode loading corresponds to the case where the dual mode outputs route the main power (high capacity) source out.

2.3.1.1. MINIMUM DC OUTPUT REQUIREMENTS

The following table defines the minimum set of DC output characteristics required to build an Instantly Available PC. The minimum power delivery subsystem feature set supports:

- Suspend to RAM (ACPI S3 state)
- A single 3.3V PCI add-in or motherboard integrated 3.3V wake device
- Suspend/Resume button
- ACPI controller's resume power well.

Note that in the minimum power delivery subsystem configuration, USB and other 5 volt motherboard integrated wake devices are not supported from the S3 sleeping state (i.e. no support for +5 Vdual).

Table 5. Minimum Required DC Output Requirements

Output	Standby Mode Min.	Standby Mode Max.[4]	Normal Mode Min.[5]	Normal Mode Green[1]	Normal Mode Max.[2]	Normal Mode Peak[3]
+3.3 Vdc	-	-	0.0 A	1.0 A	9.2 A	
+3.3 Vdual	0.0 A	0.70 A	0.5 A	1.0 A	3.0 A	-
+3.3 Vsby	0.0 A	0.25 A	0.25 A	0.25 A	0.25 A	-
+5 Vdc	-	-	0.5 A	1.4 A	16.0 A	18 A
+5 Vdual	0.0 A	0.0 A	0.0 A	0.0 A	0.0 A	-
+12 Vdc	-	-	0.05 A	0.4 A	1.4 A	4 A
-12 Vdc	-	-	0.0 A	0.0 A	0.5 A	-

Notes:

1 - Green is the test load for the efficiency requirements specified in Section 2.3.6

2 - Maximum continuous DC output power shall not exceed 145 Watts.
- Maximum peak total DC output power shall not exceed 160 Watts.
- Maximum continuos combined power on 5 Vdc, 3.3 Vdc and 3.3Vdual shall not exceed 120 Watts

3 - Peak output power not to exceed 12 seconds in duration and total DC output power must be less than 160 Watts.

4 - Maximum combined current (3.3Vdual and 3.3Vsby) during standby mode of operation shall not exceed 0.70 A. (One 3.3V PCI wake device, STR, suspend/resume button, and ACPI controller resume well)

5 - When the 5Vdc current is at the maximum the minimum 12 V current will be not less than 0.2 A.

The following table details a recommended set of DC output characteristics that, when implemented, support a fully configured Instantly Available PC. Power delivery subsystems built to the recommended specifications below support:

- Suspend to RAM (ACPI S3 state)
- Multiple I/O bus or motherboard integrated wake devices
- Suspend/Resume button
- The ACPI controller's resume power well.

Note that added support for +5 Vdual enables “off yet communicating capabilities” for USB, and other 5 volt motherboard devices.

Table 6. Recommended “Fully Featured” DC Output Characteristics

Output	Standby Mode Min.	Standby Mode Max.[4]	Normal Mode Min.	Normal Mode Green [1]	Normal Mode Max.[2]	Normal Mode Peak[3]
+3.3 Vdc	-	-	0.0 A	1.0 A	13.0 A	-
+3.3 Vdual	0.0 A	2.0 A	0.5 A	1.0 A	8.0 A	-
+3.3 Vsby	0.0 A	0.25 A	0.25 A	0.25 A	0.25 A	-
+5 Vdc	-	-	0.5 A	1.4 A	16.0 A	-
+5 Vdual	0.0 A	1.5 A	0.0 A	0.2 A	4.0 A	-
+12 Vdc	-	-	0.05 A	0.4 A	4.5 A	6.0 A
-12 Vdc	-	-	0.0 A	0.0 A	0.5 A	-

Notes:

1 - Green is the test load for the efficiency requirements specified in Section 2.3.6

2 - Maximum continuous DC output power shall not exceed 200 Watts. Maximum current on the 3.3V output will reduce the maximum 5V output below that specified such that the maximum power output will not be exceeded. Similarly, maximum current on the 5 V output reduces the 3.3V maximum current below that specified such that the maximum power output will not be exceeded.

3 - Peak +12 Vdc output power not to exceed 12 seconds in duration and total DC output power must be less than 220 Watts.

4 - Maximum continuous DC output power during standby mode of operation shall not exceed 15 Watts.

The following table describes loading conditions. Condition 1 assumes that the system supports mostly 5V wake up devices. The Condition 2 assumes that all wakeup devices except USB are powered by 3.3 V

Table 7. Loading Conditions for 3 Watt Efficiency Measurements

Output Voltage	+5 Vdual (if supported)	+3.3 Vsby and +3.3 Vdual
Condition 1	0.5 A	0.15 A
Condition 2	0.1 A	0.75 A

2.3.2. DC VOLTAGE REGULATION REQUIREMENTS

The DC output voltages must remain within the voltage ranges specified in Table 8 when PW-OK is true and Table 9 when DLPW-OK is true. Regulation of the +3.3 Vsby, +3.3 Vdual and +5 Vdual output voltages shall be maintained within the limits specified in Table 8 during the transitions between Normal mode of operation and Standby mode of operation as described in Section 2.3.1 above.

The DC voltage regulation limits include:

- DC output load ranges as specified in Section 2.3.1
- DC output ripple/noise as specified in Section 2.3.3
- DC output initial voltage set point
- DC output cross regulation

- Operating over temperature range specified
- AC input variation and drop out as specified in Section 2.2 and 2.3.4

Table 8. Normal Mode DC Output Voltage Regulation

Output	Min.	Nom.	Max.	Range
+3.3 Vdc	+3.135 V	+3.30 V	+3.465 V	±5%
+3.3 Vdual	+3.135 V	+3.30 V	+3.465 V	±5%
+3.3 Vsby	+3.135 V	+3.30 V	+3.465 V	±5%
+5 Vdc	+4.750 V	+5.00 V	+5.250 V	±5%
+5 Vdual	+4.750 V	+5.00 V	+5.250 V	±5%
+12 Vdc	+11.40 V	+12.00 V	+12.60 V	±5%
-12 Vdc	-10.80 V	-12.00 V	-13.20 V	±10%

Table 9. Standby Mode DC Output Voltage Regulation

Output	Min.	Nom.	Max.	Range
+3.3 Vdual	+3.135 V	+3.30 V	+3.465 V	±5%
+3.3 Vsby	+3.135 V	+3.30 V	+3.465 V	±5%
+5 Vdual	+4.750 V	+5.00 V	+5.250 V	±5%

Note: The voltage regulation limits DO include DC Output Noise/Ripple noted in Section 2.3.3 and NOT the voltage deviation due to DC load changes that are covered in Section 2.3.5.

2.3.3. OUTPUT RIPPLE/NOISE

The recommended output ripple/noise characteristics are detailed in Table 10 should be met throughout the load range specified in Section 2.3.1 and under all input voltage conditions as specified in Section 2.2. This recommendation applies to both normal and standby modes of operation.

Ripple and noise are defined as periodic or random signals over frequency band of 10 Hz to 20 MHz. Measurements shall be made with an oscilloscope with 20 MHz bandwidth. Outputs shall be bypassed at the output connector with a 0.1µF ceramic disk capacitor and a 10 µF electrolytic to simulate system loading. See Figure 3 below.

Table 10. DC Output Noise / Ripple

Parameter	Range	Max.
+3.3 Vdc	1.5 %	50 mVpp
+3.3 Vdual	1.5 %	50 mVpp
+3.3 Vsby	1.5 %	50 mVpp
+5 Vdc	1 %	50 mVpp
+5 Vdual	1 %	50 mVpp
+12 Vdc	1 %	120 mVpp
-12 Vdc	1 %	120 mVpp

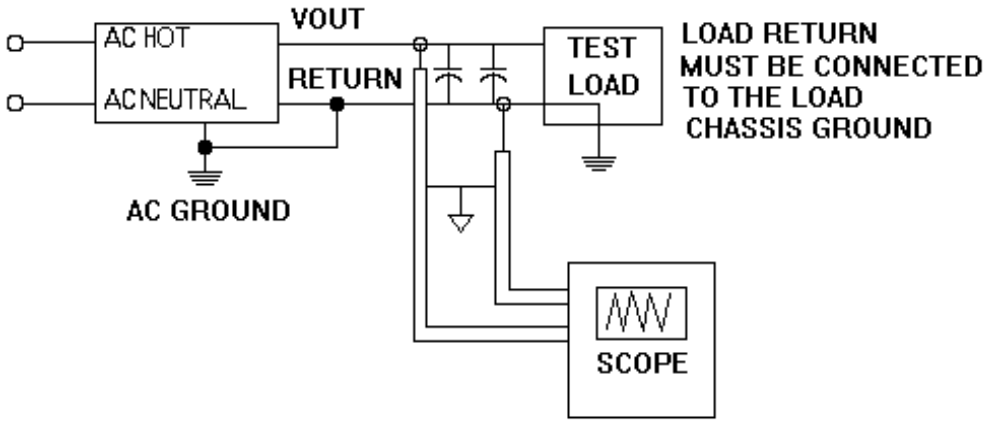

Figure 3. Differential Noise Test Setup

2.3.4. VOLTAGE HOLD-UP TIME

The power delivery subsystem shall maintain output regulation per Section 2.3.2 for a loss of input power at the low-end of the nominal input voltage range (Low = 100 or 200 VAC RMS, 47 Hz) at maximum output load as specified in Section 2.3.1 for a minimum of 17 ms. The measurement shall be made from the point at which conduction of input current ceases (AC power interrupt) to the point at which the output voltage drops below the static regulation envelope specified in Section 2.3.2.

2.3.5. OUTPUT TRANSIENT RESPONSE

The output voltage shall remain within the voltage range specified in Table 11 below for instantaneous changes in load. The load step shall apply over the full range of values specified in Section 2.3.2. The transient voltage response limits shall be maintained over the AC input range defined in Section 2.2 and all steady state temperature and operating conditions. The transient voltage limits include the voltage regulation requirements described in Section 2.3.2. The voltage shall recover to be within the regulation band specified in Section 2.3.2 within 2 ms following an instantaneous load change. The transient response measurements shall be made with a load step repetition rate varied over the full range of 50 Hz to 3333 Hz. The load slew rate shall not be greater than 0.40A/µs nor less than 0.1A/µs. The outputs not under test shall be loaded at the minimum value specified in Section 2.3.2. The load step values specified in Table 11 are defined as the maximum. In case when the current capacity is lower then specified in Table 11 the load step should be defined as the 80 % of maximum current.

Table 11. DC Output Transient Response

DC Output	Load Step	Min.	Nom.	Max.	Range
+3.3 Vdc	3.0 A	+3.135 V	+3.30 V	+3.465 V	±5%
+3.3 Vdual	2.0 A	+3.135 V	+3.30 V	+3.465 V	±5%
+3.3 Vsby	0.25 A	+3.135 V	+3.30 V	+3.465 V	±5%
+5 Vdc	5.0 A	+4.750 V	+5.00 V	+5.250 V	±5%
+5 Vdual	1.5 A	+4.750 V	+5.00 V	+5.250 V	±5%
+12 Vdc	2.0 A	+11.40 V	+12.00 V	+12.60 V	±5%
-12 Vdc	0.5 A	-10.80 V	-12.00 V	-13.20 V	±10%

2.3.6. CONVERSION EFFICIENCY RECOMENDATIONS

The conversion efficiency of the power delivery subsystem should be within the range specified in Table 12 below and should be met over the AC input range defined in Section 2.2, under the load conditions defined in Section 2.3.1.

Efficiency is defined as the ratio of total DC output power divided by the total AC input power.

Table 12. Power delivery subsystem Efficiency

Parameter	Minimum Efficiency
Normal Mode Max load	65 %
Normal Mode Green load	50 %
Standby Mode Max load	35 %
3 Watt Efficiency Load (see Table 7)	35 %

A minimally configured Instantly Available PC (STR, a single 3.3V PCI wake device, suspend/resume button, and ACPI resume well) is estimated to consume between 2-3W. The system power dissipation is dependent upon the type of memory used in the system, the number of memory modules, system indicators and wakeup devices. Note that with 2-3W required on the system side, to achieve 5W or less from the wall the conversion efficiency for the Standby Max and 3 Watt Efficiency loads would need be at least 60%. For example, if the system requires 2.5 Watts while in the sleeping state, the conversion efficiency would need to be at least 50% to keep the input power to less than 5 Watts.

2.3.7. OVERSHOOT AT TURN-ON / TURN-OFF

Any overshoot upon the application or removal of the input voltage or the PS-ON#, DUAL-ON# signals under the conditions specified in Section 2.2 shall be less than 10% above the initial set voltage. No voltage of opposite polarity shall be present on any output during turn-on or turn-off.

2.3.8. SEQUENCING

The 3.3 Vdc outputs shall track the +5 Vdc outputs and there shall not be greater than 0.5 volts difference between them during turn-on and turn-off of the outputs. It is preferred that the 3.3 Vdc outputs be slightly lower than the 5 Vdc outputs during turn-on and turn-off. This applies to both the main and the dual outputs. In addition, if both the main and the dual outputs are turning on at the same time, such as after a power failure or fault condition, then they shall track each other and there shall not be greater than 0.5 volts difference among them.

2.3.9. MONOTONICITY AT TURN-ON

The outputs of the power delivery subsystem shall rise monotonically. At no time during turn-on of any of the outputs shall the derivative of the output voltage change sign until the voltage enters the regulation band defined in Section 2.3.2.

2.3.9.1. TURN ON/OFF DELAY

The output voltages shall settle to a point within the range specified in Section 2.3.2 above within 1.0 second after power is applied to the unit or the PS-ON# signal is activated (driven low). The DC outputs must rise from 20% of their nominal output level to within the regulation band while loaded as specified in Section 2.3.1

2.3.10. CLOSED LOOP STABILITY

The vendor shall provide proof of unit closed-loop stability with local and remote sensing through the submission of Bode plots and/or root-locus test data for all regulated outputs. Closed-loop stability must be ensured at all loads specified in Section 2.3.1 and over the input voltage range specified in Section 2.2 above.

2.3.12. STANDBY OUTPUT

The +3.3 Vsby output is always present when the power delivery subsystem is connected to a source of AC voltage as defined in Section 2.2.

2.4. PROTECTION

2.4.1. OVER VOLTAGE PROTECTION

The power delivery subsystem shall provide latch-mode over voltage protection as defined in Table 13. The power delivery subsystem shall latch off if the output voltages exceed the threshold defined in Table 13.

Table 13. Over Voltage Protection

Parameter	Min.	Nom.	Max.	Unit
+3.3 Vdc	3.70	4.00	4.40	V
+3.3 Vdual	3.70	4.00	4.40	V
+5 Vdc	5.58	6.00	6.82	V
+5 Vdual	5.58	6.00	6.82	V
+12 Vdc	-	-	-	V
-12 Vdc	-	-	-	V

2.4.2. SHORT CIRCUIT PROTECTION

The power delivery subsystem shall withstand a continuous short-circuit to any output without damage or over stress to the unit (components, PCB traces, connectors, etc.) under the AC input conditions specified in Section 2.2 above. The maximum short-circuit current in any output shall not exceed the limits of Section 2.4.3. The power delivery subsystem may latch off during a short-circuit condition.

2.4.3. OVER CURRENT PROTECTION

Overload current applied to each tested output rail will cause the output to trip when they reach or exceed 240 VA. Each output rail shall be tested for over current protection with a minimum of 10A/s fault current ramp starting from full load

It is highly recommended that the power delivery subsystem provide over current protection as noted in Table 14 below.

Table 14. Over Current Protection

Parameter	Type	Nom.	Max.	Unit
+3.3 Vdc	OCP	-	<1.5 X (Imax + Dual Imax)	Amps
+3.3 Vdual	OCP	-	<1.5 X (Imax + Dual Imax)	Amps
+5 Vdc	OCP	-	<1.3 X Imax	Amps
+5 Vdual	OCP	-	<1.3 X 5V Imax	Amps
+12 Vdc	OCP	-	<1.5 X 12V Imax	Amps
-12 Vdc	-	-	<-2	Amps

2.4.4. RESET AFTER SHUTDOWN

If the power delivery subsystem latches into a shutdown state due to fault condition on its outputs, the power delivery subsystem shall return to normal operation only after the fault has been removed and power delivery subsystem's power-on switch has been cycled on-off.

3. MECHANICAL SPECIFICATION

As stated earlier, this document specifies the power delivery capabilities that must be supported within the platform in order to build an Instantly Available PC. These capabilities may be fully integrated into a stand alone power supply, or they could alternatively be supported in a distributed manner which would require the participation of a functionally mated power supply and PC motherboard.

The following sections provide a recommended set of mechanical specifications for a fully integrated stand alone Instantly Available PC power supply.

3.1. PHYSICAL DIMENSIONS/MARKINGS

The physical specification will be provided by the system designer. Examples include Baby AT, ATX, NLX.

3.2. ACOUSTIC NOISE REQUIREMENTS

Acoustic noise characteristics should be specified by the system designer.

3.3. AIR FLOW

The power supply must be designed to provide sufficient airflow to cool both its own internal components and integrated system components. The exact venting locations and geometry as well as fan selection for the supply will vary.

Existing standard form factor (e.g. ATX, NLX) power supplies' air flow requirements must be met for each corresponding form factor.

3.4. AC CONNECTOR REQUIREMENTS

The power supply may incorporate a manual AC input select between 90-132 Vac range and 180-264 Vac. The AC input receptacle shall conform to the requirements specified in CEE 22.6 for an IEC 320 C14 type connector.

An auxiliary AC output receptacle may be included if so desired.

3.5. DC CONNECTOR RECOMMENDATIONS

The following subsections detail the recommended connector specifications for a fully integrated Instantly Available PC power supply. The connectors specified in this section are given as an example. Other connector may also be used to meet specific requirements or to reduce cost.

3.5.1. LOGIC CONNECTORS

Tables 15 and 16 show the connector pinouts for the main outputs. There are two connectors, P1 and P2, to deliver the power supply output voltages and control signals to the motherboard.

As the example the main connector P1 is a Molex connector PN 39-01-2240. This connector mates with motherboard connector PN 39-29-9242. (same style connector as used in ATX power supplies with 24 pins instead of 20 pins). All wires are 18 AWG and the cable length external to the chassis is 250 mm minimum.

Example of a connector P2 is a small connector with 0.1 inch center dual row pins. The wires may be either 26 AWG ribbon cable or 24 AWG wires. The connector is rated at 1A per pin.
The P2 power delivery subsystem connector is Molex 22-55-3201. The P2 connector from the power delivery subsystem mates with the motherboard connector Molex 70246-2021

Table 15. Connector P1 Pinout

18 AWG Wire	Signal	Pin	Pin	Signal	18 AWG Wire
Gray	+5 Vdual	13	1	COM	Black
White	+3.3 Vdual	14	2	COM	Black
White	+3.3 Vdual	15	3	COM	Black
	Reserved	16	4	COM	Black
Orange	+3.3 V	17	5	COM	Black
Orange	+3.3 V	18	6	COM	Black
Orange	+3.3 V	19	7	COM	Black
	Reserved	20	8	COM	Black
Red	+5 Vdc	21	9	Reserved	
Red	+5 Vdc	22	10	Reserved	
Red	+5 Vdc	23	11	Reserved	
Red	+5 Vdc	24	12	+12 Vdc	Yellow

Table 16. Connector P2 Pinout

24 AWG Wire or ribbon cable	Signal	Pin	Pin	Signal	24 AWG Wire or ribbon cable
	Reserved	1	2	PS-ON#	Green
Orange	+3.3 Vsby	3	4	Dual-ON#	Yellow
White	3.3 Vdual sense	5	6	COM	Black
Black	COM	7	8	COM	Black
Brown	3.3 V sense	9	10	Reserved	
Violet	DLPW-OK	11	12	Reserved	
Gray	PW-OK	13	14	COM	Black
Blue	-12 VDC	15	16	FANRPM	White
Black	COM	17	18	FANCON	Yellow
	Reserved	19	20	Reserved	

Note: Color cable requirement does not have to be met if the ribbon cable is used.

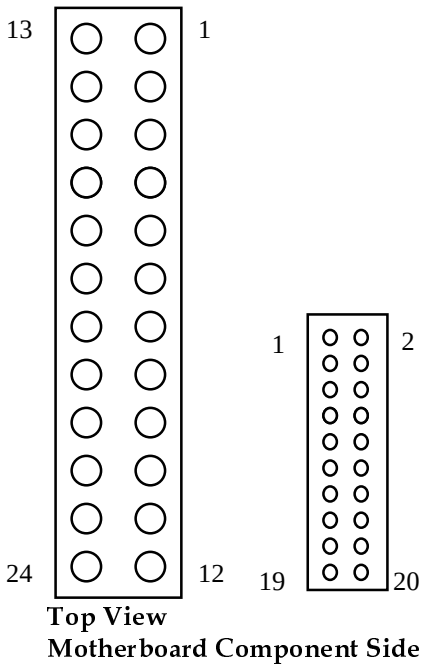

Figure 4. Main power connectors P1 and P2 configuration

3.5.2. PERIPHERAL CONNECTORS

These outputs provide power to the disk drives and other peripherals in the system. The minimum cable length is 300 mm for P4, P5, P6 and P7. P8 is daisy chained from P5 and P9 is daisy chained from P7. The length of the daisy chain cables is 100 mm minimum.

Table 17. Peripheral Connector (P3-P8) Pinouts

P3, P4, P5, P6 AMP 1-480424-0 or MOLEX 8981-04P or equiv.

Pin	Signal	18 AWG Wire
1	+12 Vdc	Yellow
2	COM	Black
3	COM	Black
4	+5 Vdc	Red

P7, P8 AMP 171822-4 or equivalent

Pin	Signal	26 AWG Wire
1	+5 Vdc	Red
2	COM	Black
3	COM	Black
4	+12 Vdc	Yellow

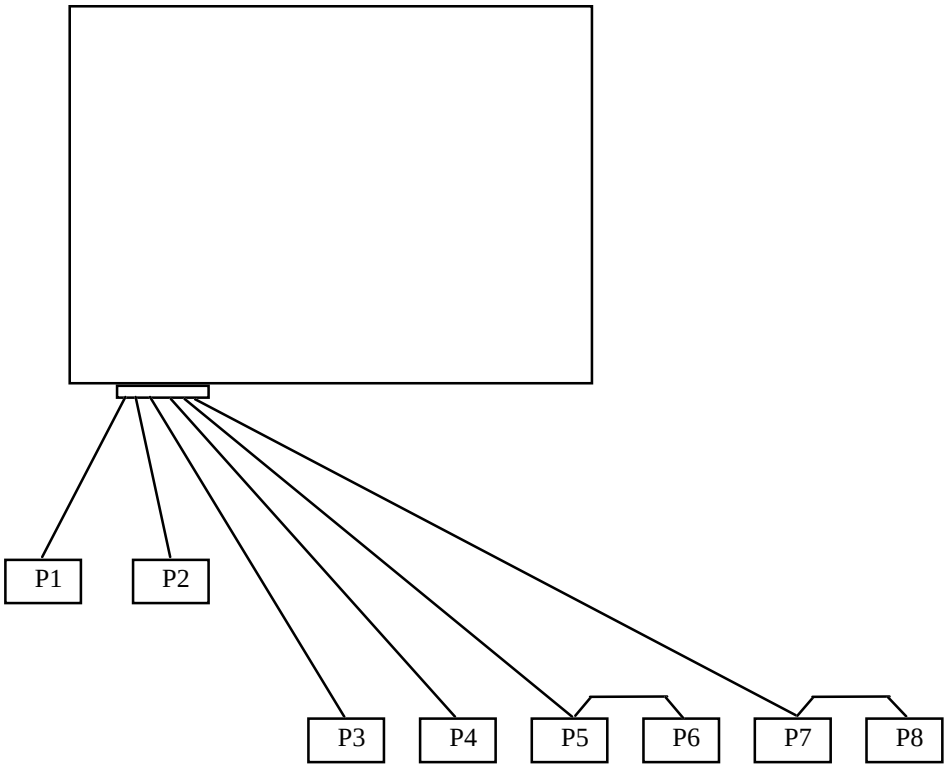

Figure 5. Typical Connector Harness Assembly

3.6. ACCESSIBILITY

There shall be no internal parts accessible externally on the power supply.